Attenuation Compensation in Distributed Amplifier Design

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Abstract—**A high-gain common-gate FET can present at its drain a broad-band impedance characterized by a (frequency-dependent) negative resistance and a capacitance. This is examined both theoretically and experimentally. Loading the input and/or the output lines of a distributed amplifier with this circuit reduces the signal losses, leading to an increase in the allowed number of active devices with a consequent increase in the gain–bandwidth and gain–maximum frequency products. The cascode circuit, a related loss reduction network, is also evaluated because of its use in distributed amplifiers. Several designs employing the common-gate FET loss-compensating circuit and/or the cascode amplifying circuit are compared to a conventional distributed amplifier optimized for gain–bandwidth product. Simulated gain–maximum operating frequency product increases of 27 to 245 percent over that of the optimized conventional distributed amplifier are shown. The increase in single-stage amplifier gain provided by this technique often results in (proportionally) higher maximum output power.**

I. Introduction

IMPROVEMENT in the gains, power outputs, and bandwidths of recent monolithic distributed amplifiers (DA's) [1]–[11] has been prevented by three factors: the input line attenuation, the output line attenuation, and the dynamic (linear) range of the input signal. The primary loss mechanisms of the two lines are the transistor loadings rather than the (microstrip) interconnecting line losses. Thus, all three performance-limiting factors may be addressed by careful transistor design. Advanced transistor design is important for DA improvement, but is not the only means available.

This paper reports on a novel "negative resistance" (NR) circuit which lessens the line attenuations and can lead to increases in the amplifier gain–bandwidth, gain–maximum frequency, and power–frequency products. The cascode circuit, related to the NR circuit, is also discussed. An approximate stability analysis of the (four-port) DA is presented. Lastly, the enhanced performance promised by the NR circuit is indicated.

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II. Conventional Distributed Amplifier Analysis

A typical conventional DA circuit consists of periodically spaced field-effect transistors (FET's) which are interconnected by electrically short, high-impedance microstrip lines [12]. A DA design may be qualitatively described as a set of artificial input and output lines coupled by (FET) transconductances.

In this paper "conventional" refers to those DA's for which the amplifying element is a common-source FET and for which no active circuit loss compensation is used. All other DA's are said to be "unconventional" or "modified."

Analytical studies of a simplified conventional DA have been completed, yielding insight into design fundamentals and trade-offs [12]–[14]. One important conclusion is that the line attenuation parameters A_g and A_d control the gain and bandwidth. Highlights of the analyses follow below.

The simplified transistor equivalent circuit (shown in Fig. 1) applied to the DA circuit of the above studies results in the following gain and attenuation expressions:

$$A = \frac{g_m \cdot \sqrt{R_{01} R_{02}} \cdot \sinh\left[n(A_g - A_d)/2\right] \cdot \exp\left[-n(A_g + A_d)/2\right]}{2\sqrt{1+(X_k)^2\left[\frac{\omega_c}{\omega_g}\right]^2}\sqrt{1-(X_k)^2} \cdot \sinh\left[(A_g - A_d)/2\right]} \quad (1)$$

$$A_g = \frac{(\omega_c/\omega_g)\cdot(X_k)^2}{\sqrt{1-\left\{1-\left[\omega_c/\omega_g\right]^2\right\}\cdot(X_k)^2}} \quad \text{(nepers/section)} \quad (2)$$

$$A_d = \frac{\omega_d/\omega_c}{\sqrt{1-(X_k)^2}} \quad \text{(nepers/section)} \quad (3)$$

where $\omega_g = 1/(R_i C_{gs})$, $\omega_c = 2/\sqrt{L_g C_{gs}} = 2/\sqrt{L_d C_{ds}}$, $\omega_d = 1/(R_{ds} C_{ds})$, $X_k = \omega/\omega_c$, $R_{01} = \sqrt{L_g/C_{gs}}$, and $R_{02} = \sqrt{L_d/C_{ds}}$. The variable A represents the amplifier voltage gain per stage. The variables A_g and A_d are the input line and output line attenuation terms, respectively. Physically, R_{01} and R_{02} represent the low-frequency input and output line image impedances. The term X_k is a frequency normalized to the LC structure cutoff frequency. Lastly,

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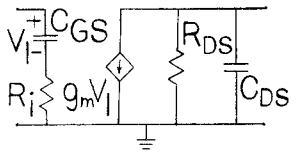

Fig. 1. Simplified common-source FET equivalent circuit

ω_g and ω_d are the FET input and output impedance corner frequencies, respectively.

From (2) and (3), one notes that A_d is frequency invariant until nearing the LC cutoff frequency ($X_k = 1$), whereas A_g varies approximately with the square of frequency. Thus, at low frequencies A_d dominates the DA response while A_g begins to play a role at midband. The dc gain expression given below in (4), derived from (1)–(3), shows the performance limitations imposed by A_d:

$$\text{dc gain} = A_0 = \frac{g_m \cdot \sqrt{R_{01}R_{02}}\left[1-\exp\{-nA_d(0\text{ Hz})\}\right]}{4\sinh\left[A_d(0\text{ Hz})/2\right]}$$

$$= A_0(n). \tag{4}$$

The maximum dc gain is inversely proportional to $\sinh[A_d(0\text{ Hz})/2]$. Lower output loss FET's, higher image impedances, and/or higher gain FET's are necessary to extend the dc gain limits in the conventional DA. At high frequencies, the impact of the input line attenuation term A_g is felt. Reduction of A_g allows higher DA operation frequencies. Equations (1)–(4) indicate several design trade-offs which have been addressed in the literature.

III. Negative Resistance Loss Compensation

Examinations of (1) indicate DA gain improvement with decreasing section attenuation factors A_g and A_d. "Active" impedances placed along the loaded lines can lessen or overcome the attenuation (see Appendix, Fig. 11). Active impedances, characterized by frequency-dependent reactances and negative resistances, reduce the net attenuation terms by compensating the signal losses dominated by the positive transistor resistances R_t and R_{ds}. Thus "negative resistance (NR) compensation" aptly describes the concept.

The impact of NR compensation is twofold. First, by lessening the attenuation on one or both of the lines, more sections can be usefully added to a single DA stage. The increased single-stage gain permits a proportional maximum output power increase in those amplifiers limited by the dynamic (linear) range of the input signal. The maximum amplifier output power is then given by $G_p \cdot P_{\text{in(max)}}$, which is proportional to the single-stage amplifier power gain G_p and to the (limited) maximum input signal strength $P_{\text{in(max)}}$. The second impact of NR loss compensation is an extension of the bandwidth. Broad-band loss compensation on either DA line permits significant bandwidth increases.

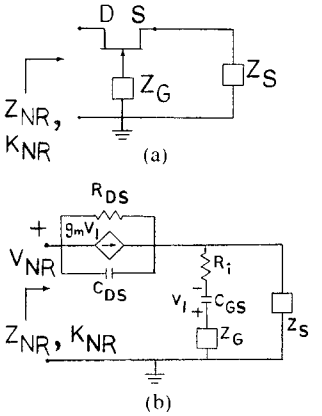

Fig. 2. A common-gate FET circuit including impedances Z_g and Z_s, both encountered in the FET biasing circuit. (a) Circuit schematic. (b) Simplified equivalent circuit

IV. The Common Gate Negative Resistance Circuit

The schematic and the simplified circuit model of a type of common-gate FET circuit are found in Fig. 2. When driven at its drain terminal, such a circuit can provide a negative resistance and a capacitance over a wide band of frequencies. Loading the artificial transmission lines of a DA with this circuit results in a considerable reduction in attenuation with minimal dispersion. Equation (5) shows the resulting input impedance, Z_{nr}:

$$Z_{nr} = \frac{R_{ds}}{1+j\omega C_{ds}R_{ds}}\left[1+\frac{g_m Z_s}{1+j\omega C_{gs}(R_t+Z_s+Z_g)}\right] + \frac{Z_s\left[1+j\omega C_{gs}(R_t+Z_g)\right]}{1+j\omega C_{gs}(R_t+Z_s+Z_g)}. \tag{5}$$

The impedances Z_g and Z_s model the bias and termination loads. Assuming these to be passive, only the voltage-dependent current generator (via the term g_m) contributes to the formation of an active impedance Z_{nr}. The interplay of the elements in Fig. 2 can be determined directly from (5). However, insight into the nature of Z_{nr} is more readily obtained by examining Z_{nr} under a few specific conditions, namely low-frequency excitation and the case of infinite source terminating impedance Z_s.

At very low frequencies, the common-gate circuit provides insufficient loss compensation. This is seen by allowing the frequency to approach zero in (5), resulting in

$$Z_{nr}(f \to 0\text{ Hz}) = R_{ds}(1+g_m Z_s) + Z_s. \tag{6}$$

Assuming the phase of g_m to be given by $-\omega\tau$ (τ is the FET transit time), then only in the case of highly reactive source impedance loading could $\text{Re}\{Z_{nr}\}$ be negative at low frequencies. The dependence of Z_{nr} on the large drain-to-source resistance R_{ds} indicates that NR circuits load the DA lines minimally at low frequencies.

A second specific condition to examine is when the source termination Z_s becomes infinite. Computer simulations indicate that a large $|Z_s|$ is appropriate for NR compensation across very broad bands. Small values of

$|Z_s|$ tend to decrease the available NR loss compensation because a small, nonresonant source load $|Z_s|$ degrades the voltage division of the input signal across the FET gate-to-source capacitor. The result is a decreased normalized current generator drive ratio $|V_1/V_{nr}|$. When $|Z_s|$ approaches infinity, (5) simplifies to the form

$$Z_{nr} = \frac{R_{ds}}{1+j\omega C_{ds}R_{ds}} + \frac{1}{j\omega C_{gs}} + R_i + Z_g + \frac{g_m R_{ds}}{j\omega C_{gs}[1+j\omega C_{ds}R_{ds}]}. \quad (7)$$

The first four terms of (7) are passive in nature, while the fifth term (involving g_m) provides the negative resistance. The real part of the fifth term is

$$\mathrm{Re}\left[\frac{g_m R_{ds}}{j\omega C_{gs}[1+j\omega C_{ds}R_{ds}]}\right] = -\frac{g_m R_{ds}/(\omega_d C_{gs})}{(1+j\omega/\omega_d)(1-j\omega/\omega_d)} \quad (8)$$

where, as before, $\omega_d = 1/(R_{ds}C_{ds})$. For $\omega \geq 2\omega_d$, the negative resistance term of (8) decreases approximately as $1/\omega^2$. Consequently, one can expect an upper frequency to exist at which the net resistance $\mathrm{Re}\{Z_{nr}\}$ becomes positive. Computer simulations of a Honeywell monolithic 0.25×100 μm MODFET equivalent circuit show that the net negative resistance $\mathrm{Re}\{Z_{nr}\}$ extends beyond 70 GHz with various source terminating loads. This FET is discussed later.

Low-gain FET's provide insufficient loss compensation for practical use as common-gate NR circuits. In fact, very low gain FET's cannot overcome the losses attributed to the circuit components R_{ds}, R_i, and Z_g. This is because the NR term of (8) is proportional to g_m. In contrast, as C_{gs} decreases, the NR circuit compensation increases via a larger reflection. This effect may be explained by voltage division concepts: higher impedance gate-to-source capacitances experience greater $|V_1/V_{nr}|$ ratios and thus provide larger current generator drive.

Experimental measurements of the common-gate circuit indicate useful broad-band NR behavior. The de-embedded scattering parameter measurement of S_{11} in Fig. 3 is taken at the drain terminal of a Honeywell common-gate MODFET. Above 18 GHz this 0.25×100 μm MODFET, modeled by the circuit of Fig. 4, presents an impedance for which the real part is negative. The common-gate measurements compare well with FET model simulations, allowing one to implement a NR circuit model during the DA design procedure. (This is to be expected considering (i) the physical implications of the modeling process and (ii) the excellent results obtained by LaRue *et al.* [4] in their extensive FET modeling procedure, for which a single circuit was fitted to common-gate, common-drain, and common-source measurements.)

Computer simulations predict broad bands over which the common-gate circuit provides useful loss compensation. The simulations are based upon internal (monolithic version) MODFET models scaled from the 0.25×100 μm

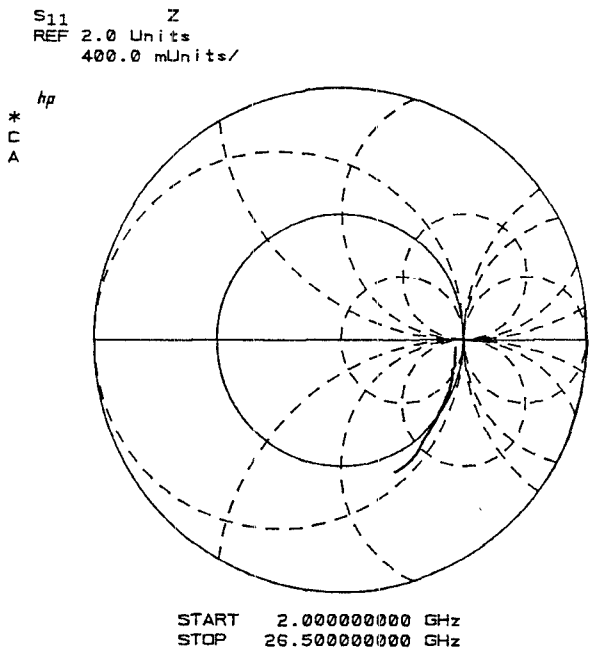

Fig. 3. Drain reflection measurement of a 100×0.25 μm^2 Honeywell MODFET in a common-gate configuration. Above 18 GHz, a negative resistance is displayed.

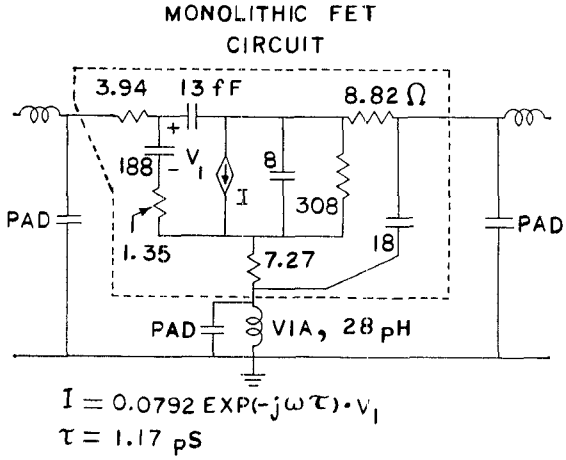

Fig. 4. Equivalent circuit model of the Honeywell 100×0.25 μm^2 MODFET (shown in a common-source configuration). Bonding pad capacitances and wire (and via hole) inductances complicate the basic monolithic circuit model.

MODFET equivalent circuit in Fig. 4. (Fig. 4 includes the hybrid circuit bond pad capacitances and bond wire inductances.) The capacitances, the transconductance, and the conductances scale in proportion to the FET gate width. The simulated scattering parameters of Fig. 5 also describe the common-gate circuit characteristics. By terminating port 2 with a reflective load K_1, one obtains a net input reflection coefficient, K_{in}, at port 1:

$$K_{in} = S_{11} + S_{12}S_{21}K_1/(1-S_{22}K_1). \quad (9)$$

The nonzero $S_{12}S_{21}$ term obtained from the parameters of Fig. 5 indicates that source terminations can influence the NR behavior, consistent with (5) and (6). The simulated net input reflection curves of Figs. 6 and 7 demonstrate this. Fig. 6 shows the useful broad-band NR compensation

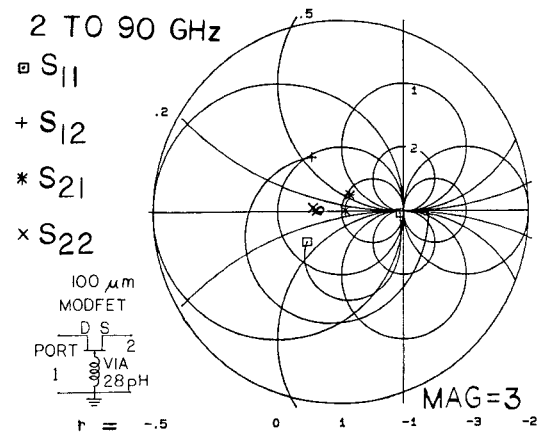

Fig. 5. (TOUCHSTONE) Simulated scattering parameters of the Honeywell (monolithic) MODFET common-gate circuit.

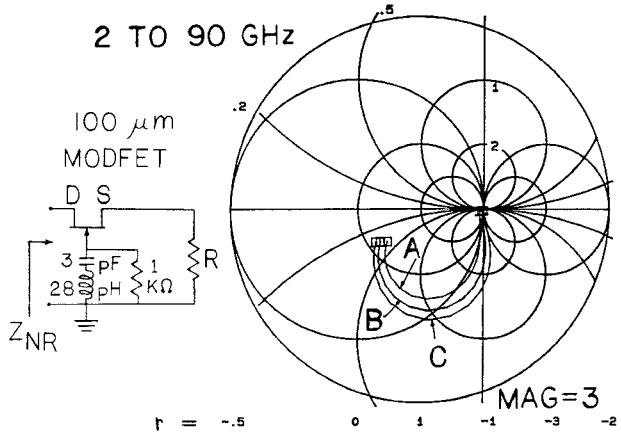

Fig. 6. (TOUCHSTONE) Simulated reflections of the Honeywell common-gate MODFET using resistive source terminations A gate biasing circuit is included. Curve A: $R = 50\ \Omega$ Curve B: $R = 150\ \Omega$. Curve C: R approaches infinity.

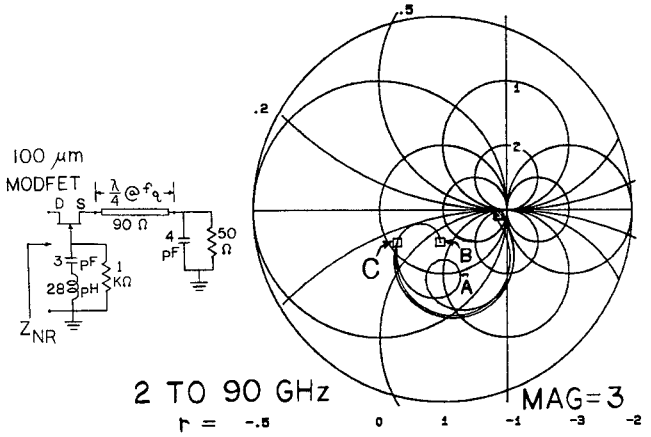

Fig. 7. (TOUCHSTONE) Simulated reflections of the Honeywell common-gate MODFET employing a quarter wave source bias circuit and a gate bias circuit. Curve A: $f_q = 30$ GHz. Curve B: $f_q = 45$ GHz. Curve C: $f_q = 90$ GHz.

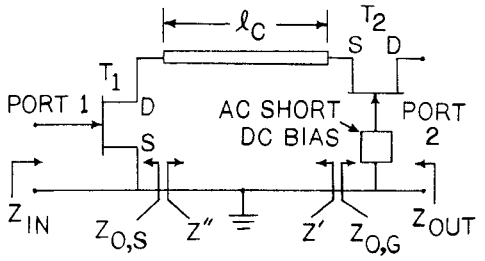

Fig 8. A cascode circuit, consisting of a common-source FET, a short transmission line, and a common-gate FET.

available using resistive source terminations. In the simulations of Fig. 7 the source termination is formed by a quarter-wavelength (at band center) transmission line terminated by a large capacitance. This allows one to provide FET biases without power losses in bias resistors while maintaining very broad band NR compensation.

V. The Cascode Circuit: Its Use in Distributed Amplifiers

With regard to output line loss compensation, incorporating the common-gate NR circuit with the primary amplifying circuit (a common-source FET) is advantageous in several respects. The source-to-drain signal transmission of the common-gate FET (S_{12} of Fig. 5) is greater than unity magnitude across a large frequency span, whereas the reverse transmission (S_{21} of Fig. 5) remains small. Therefore, connecting the drain of a common-source FET to the source of the common-gate FET can improve the net signal amplification and the reverse isolation. The resulting amplifying circuit, depicted in Fig. 8, is the cascode. The short transmission line, referred to as the cascode line, separates the two transistors, altering the cascode forward gain and the output impedance because of the impedance transformations from $Z_{o,g}$ to Z'' and $Z_{o,s}$ to Z', respectively. High gain cascodes display negative resistance output impedances at moderate to high frequencies because of the common-gate FET output block.

A development of the cascode circuit within the context of loss compensation has been given. However, this circuit is not new to the distributed configuration. Others have reported the use of dual-gate FET's and cascodes in DA applications (cf. [2], [4], [11]), often citing the increased output impedance over that of a common-source FET for increased gain and bandwidth. As trends continue toward higher frequencies and as higher gain FET's are developed, the negative resistance output properties of the cascode must be more closely evaluated in the overall DA design. Since the cascode output, a common-gate FET, is a type of attenuation-compensating network, cascode DA's are included in the DA configuration comparisons in Section VII.

VI. Stability Considerations

For stability, one desires the net input reflection coefficients at the four DA ports to have less than unity magnitude. This translates to four series of conditions, each involving three port terminations and the 16 DA S parameters. Such analyses are very complex and not easily adapted to graphical techniques. In addition, these extensive analyses may be of little practical use with DA's

because of the extreme S parameter variations across the wide bands of operation, especially the phase variations.

A simplified analysis provides insight into the stability conditions. Here the net input reflection at the jth port of the DA, $K_{\text{in},j}$, is approximated by

$$K_{\text{in},j} = S_{jj} + \sum_{\substack{m=1 \\ m \neq j}}^{4} S_{mj} K_{L,m} S_{jm}. \tag{10}$$

The term S_{kl} is a DA four-port scattering parameter and $K_{L,m}$ is the reflection coefficient of the mth port termination. Stable, nonoscillatory behavior is maintained when $|K_{\text{in},j}|$ is less than unity for each of the four ports.

When the phases of the four addends in (10) are equal, the largest reflection magnitude $|K_{\text{in},j}|$ occurs. This constructive addition of reflection terms leads to the four most stringent stability conditions:

$$|K_{\text{in},j}| = |S_{jj}| + \sum_{\substack{m=1 \\ m \neq j}}^{4} |S_{mj} K_{L,m} S_{jm}| \overset{\text{set}}{<} 1, \qquad j = \{1,2,3,4\}. \tag{11}$$

Assuming the four-port scattering parameters to be given, (11) establishes limitations on the set of port termination tolerances $\{|K_{L,m}|\}$ which are based upon the transmission factors $\{|S_{mj}S_{jm}|\}$. The stability criteria have been formulated. The question remains how one specifies port termination tolerances which guarantee stable, insensitive amplifier operation. From the system standpoint, a uniform restriction on port terminations is desirable. This leads to the specification of a maximum termination reflection coefficient, $K_{L,\max}$, for all four ports (of the DA):

$$K_{L,\max} \geq |K_{L,j}|, \qquad j = \{1,2,3,4\}. \tag{12}$$

A tolerance is derived from (11) and (12):

$$K_{L,\max} = \min\left[\left[1 - |S_{jj}|_{\max}\right] \Big/ \left(\sum_{\substack{m=1 \\ m \neq j}}^{4} |S_{mj} S_{jm}| \right) \right] \tag{13}$$

for $j = \{1,2,3,4\}$. When all four ports are terminated by loads with reflection magnitudes less than $K_{L,\max}$, stable, nonoscillatory behavior is maintained. Therefore the term $K_{L,\max}$ is a stability criterion. Equation (13) indicates stability improvement with decreasing $\{|S_{jj}|\}$ and $\{|S_{mj}S_{jm}|\}$. Because the trends of the four-port scattering parameters vary with frequency, it is desirable to calculate a few values of $K_{L,\max}$ based upon midband and upper band edge S parameters.

The transistor characteristics and the DA configuration play dominating roles in determining $K_{L,\max}$. The transistor gains, isolations, and parasitic loading impedances influence the set of transmission factors $\{S_{jm}S_{mj}\}$, which in turn govern $K_{L,\max}$. Similarly, the DA configuration strongly influences the set $\{S_{jm}S_{mj}\}$. Amplifiers employing input line compensation display an increased $|S_{21}S_{12}|$ term. Likewise, DA's with output line compensation (via cascodes) possess an increased $|S_{43}S_{34}|$ value. Not only are the line transmission factors affected by loss compensation, but other pairs of transmission magnitudes may be increased.

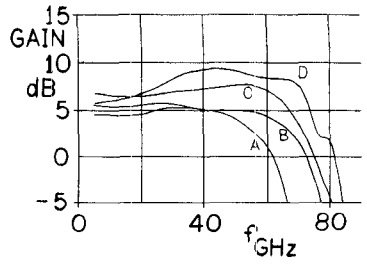

Fig. 9. Frequency response of the four-section DA's Curve A: Conventional configuration. Curve B: (Input line) compensated configuration. Curve C: Cascode-based configuration. Curve D: (Input line) compensated cascode configuration.

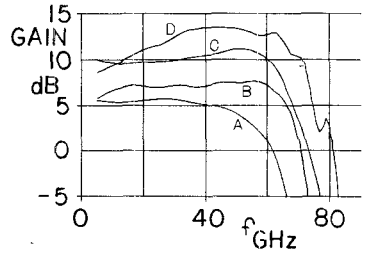

Fig. 10. Response of four DA's. Curve A: Conventional configuration (four sections). Curve B: (Input line) compensated configuration (eight sections). Curve C: (Input line) compensated cascode configuration (eight sections).

Stability Example

A cascode DA with the following midband characteristics is used for stability calculations: S_{41} (dB) = S_{22} (dB) = 10, S_{14} (dB) = S_{23} (dB) < −25, S_{11} (dB) = S_{22} (dB) < −15, S_{44} (dB) = S_{33} (dB) < −15, $|S_{21}| = |S_{12}| = 0.7$, $|S_{43}| = |S_{34}| = 1.2$, S_{31} (dB) = S_{42} (dB) < 7, and S_{13} (dB) = S_{24} (dB) < −30. Using (11)–(13), a value of $K_{L,\max} = 0.487$ is found, which guarantees stable, nonoscillatory operation at midband frequencies.

VII. A Comparison of Circuit Designs

Seven millimeter-wave DA's were simulated and optimized with the aid of the TOUCHSTONE computer program. Each design employs the scaled equivalent circuits of Honeywell 0.25×100 μm monolithic MODFET's (Fig. 4). A maximized performance four-section conventional design serves as the basis for comparison. In Fig. 9 the gains of the conventional DA and of three loss compensated DA's employing four sections are given. Three loss compensated DA's employing eight sections are compared to the conventional, four-section DA in Fig. 10. The small sizes of the transistors comprising the seven amplifiers were in part responsible for the very high frequencies achieved. The Appendix contains complete details of the seven amplifier designs.

A. Gains and Bandwidths

Curve A of Fig. 9 displays the conventional DA frequency response, a gain of 5.25 dB to 45 GHz. This

TABLE I
PASSBANDS, RETURN LOSSES, AND GAINS OF THE EXAMPLE DISTRIBUTED AMPLIFIERS (FIGS. 9 AND 10)

Amplifier Description	Passband (GHz)	Gain (dB)	Return Losses (dB) Input	Output
Four-section conventional, curves *A*	dc–45	5.25±0.5	>14.9	14.6
Four-section compensated, curve *B* of Fig. 9	dc–60	4.85±0.5	> 8.5	>15.2
Four-section cascode, curve *C* of Fig. 9	27–62	7.18±0.5	>10 3	>14 4
Four-section compensated, cascode, Curve *D* of Fig. 9	30–62	8.88±0.5	> 7.0	>15 9
Eight-section compensated, Curve *B* of Fig. 10	10–62	7.15±0.5	> 7.4 > 9, $f < 60$	>15.3
Eight-section cascode, curve *C* of Fig. 10	35–60	10.71±0.5	>13.7	>13.3
Eight-section compensated cascode, curve *D* of Fig. 10	30–64	12 95±0.5	> 7.2	>13.9

amplifier has been maximized for gain–bandwidth product (GBWP), achieving a value of 82.4 GHz, and serves as the standard for single-stage response within this transistor family. Because the bandwidth of this amplifier equals the maximum operating frequency, the GBWP equals the gain–maximum operating frequency product (GMFP).

Curve *B* of Fig. 9 is the gain of the DA using input line compensation. The compensation consists of common-gate transistor circuits placed on the input line midway between the amplifying common-source FET's. Here the 4.85 dB gain extends to 60 GHz, resulting in single-stage GBWP and GMFP increases of 27 percent, to 104.9 GHz.

The frequency response of a cascode-based DA is found in curve *C* of Fig. 9. The 7.18 dB gain of this four-section "cascode DA" covers 27 to 62 GHz. This gives a GBWP of 80.0 and a GMFP of 141.7 GHz. The GMFP for this amplifier is 72 percent greater than that of the conventional DA. A high frequency loss was introduced into the output line of the cascode DA to stabilize the onset of the cascode NR output impedance.

Curve *D* of Fig. 9 displays the response of a cascode-based DA which is also compensated on the input line with common-gate NR circuits. This amplifier, termed the compensated cascode DA, does not provide exceptional gain flatness. Nonetheless, the 8.9 dB gain performance between 30 and 65 GHz is considerable. This represents a GBWP of 97.3 GHz and a GMFP of 180.7 GHz, improvements of 18 percent and 119 percent over those of the conventional design. The low frequency slope of curve *D* may be attributed to the onset and gradual increase of NR loss compensation from the common-gate FET's throughout this sample frequency span.

Fig. 10 is a gain comparison of the conventional, four-section DA with three compensated DA's, each using eight sections. Because NR compensation reduces attenuation, an increase in the optimum number of sections results. Hence the full advantage of NR compensation can only be realized if the number of active devices is increased. Curve *A* is the optimized conventional DA (the same DA of Fig. 9, curve *A*). Curve *B* is the frequency response of the DA which uses input line compensation only. The increase from four sections to eight accounts for the gain increase between curve *B* of Fig. 9 and curve *B* of Fig. 10. The MODFET output loss prohibits large gain increases with additional DA sections. Curve *C* of Fig. 10 is the eight-section cascode DA response. Here the usual number of DA sections in a stable design is governed by the input line attenuation. Lastly, curve *D* of Fig. 10 shows the response of the eight-section compensated cascode DA. This design shows a low frequency gain slope.

Referring to Fig. 10, the compensated DA has a 7.15 dB gain between 10 and 62 GHz, corresponding to a GBWP of 118.4 GHz and a GMFP of 141.2 GHz. These are 43 percent and 71 percent greater, respectively, than those of the conventional DA design. The eight-section cascode DA has a gain of 10.71 dB across the 35 to 60 GHz span, yielding a GBWP of 85.8 GHz and GMFP of 205.9 GHz, improvements of 4.1 percent and 150 percent over the conventional DA. The eight-section compensated cascode DA gives a GBWP equal to 151.0 GHz and GMFP equal to 284.2 GHz. These are improvements of 83 percent and 245 percent respectively.

The design procedure for the DA's of Figs. 9 and 10 involved gain optimization as well as optimization of return losses and of smooth, controlled transmissions across the DA input and output lines (S_{21} and S_{43}). These are important for stability, power performance and modular system applications. Table I provides a summary of simu-

TABLE II
COMPARISON OF MAXIMUM DA OUTPUT POWERS: PROJECTED MAXIMUM OUTPUT POWERS OF THE CONVENTIONAL DA (CURVE *A* OF FIG. 10), THE CASCODE DA (CURVE *C*), AND THE COMPENSATED CASCODE DA (CURVE *D*) ARE COMPARED TO THAT OF THE INPUT LINE COMPENSATED DA (CURVE *B*)

f (GHz)	P_{max} (Curve *B* of Fig. 10) / P_{max} (Curve *A* of Fig. 10)	P_{max} (Curve *B* of Fig 10) / P_{max} (Curve *C* of Fig. 10)	P_{max} (Curve *B* of Fig. 10) / P_{max} (Curve *D* of Fig. 10)
25	4.2	0.77	1.0
35	2.4	0.77	1.0
45	2.6	1.1	1.2
55	out of passband	1.9	1.8

lated return losses and responses of the seven amplifiers.

B. Power Considerations

The increased gains of the six NR loss-compensated DA's of curves *B*, *C*, and *D* in Figs. 9 and 10 do not necessarily lead to increased maximum output power levels. Power saturation mechanisms, especially those of cascodes and dual gate FET's, can adversely affect the allowed maximum DA input power and thereby lessen the maximum output power. Each FET has limited voltage swings across its nodes for linear performance. The circuit configuration, the component values, the input power level, and the specific location within the circuit influence the FET ac voltages. In the cascode DA, the FET ac voltages are especially sensitive to the cascode line length(s). The ac voltage constraints of the second (common-gate) cascode FET often restrict the voltage swing across the first cascode FET to less than its inherent dynamic range. Hence, input power may have to be reduced. This might explain why cascode and dual-gate DA's reported in the literature have not greatly extended output power levels despite showing improved gain–bandwidth products over conventional DA's.

A study of projected maximum output powers shows the input line compensated DA (curve *B*, Fig. 10) to surpass both the cascode DA and the compensated cascode DA (curves *C* and *D*, Fig. 10) in performance by as much as 90 percent at high frequencies (55 GHz). Power performance is summarized in Table II. The primary saturation mechanism was assumed to be the ac gate-to-source voltage swing. It must be stressed that all DA design examples in this paper were optimized for GBWP, not for maximum output power.

It appears that crucial signal saturation mechanisms must be closely examined throughout the design process to ensure maximized power output, regardless of the DA configuration. Preliminary studies do indicate that the appropriate NR loss compensated DA designs can drastically improve the maximum DA output power levels.

VIII. CONCLUSIONS

Enhanced DA frequency responses are possible by lessening or eliminating the signal losses present along the input and/or the output lines. The new loss compensation technique presented here involves a "negative resistance" circuit placed in shunt on the lossy line. That circuit, based upon a common-gate FET, has an impedance characterized by negative resistance and a capacitive reactance. Two design simulations using the NR circuit for input line loss compensation have shown GBWP and GMFP increases of 27 percent and 71 percent over those of the conventional DA design. Cascodes, amplifiers related to the negative resistance circuit, were discussed. Simulations of two cascode DA design examples predict GMFP increases of 72 percent and 150 percent beyond that of the conventional DA. Two DA simulations of loss compensation on both DA lines (via the compensated cascode DA) have shown GMFP increases of 119 percent and 245 percent. Lastly, a first-order, four-port stability analysis has been presented, yielding insight into DA loading and stability.

The use of NR loss compensation on either of the DA lines allows substantially higher single-stage gain–bandwidth product performance than the maximum product possible with conventional DA designs. The impact of this performance enhancement is twofold: improvements in the single-stage gain often promise increased maximum output power, while increases in bandwidth are desirable for modular system design.

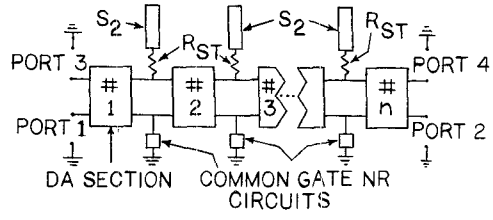

Fig. 11 The general configuration of the seven distributed amplifier (DA) design examples.

APPENDIX
DISTRIBUTED AMPLIFIER (DA) DESIGN DETAILS

The details of the seven DA designs are found in Figs. 11–14 and Tables III and IV. Fig. 11 is a generalized block diagram of the seven DA's. A typical gain section detail (DA section #k) may be found in Fig. 12. Two amplifying circuits, the common-source transistor of Fig. 13(a) and the cascode circuit of Fig. 13(b), have been used in the designs. In Fig. 14 is the common-gate negative resistance circuit. Tables III and IV list appropriate values for the circuit elements. The microstrip lines (TL_j) and open-ended stubs (S_1, S_2) have widths and lengths given in μm and denoted by 'w' and 'l', respectively. A (GaAs) substrate of

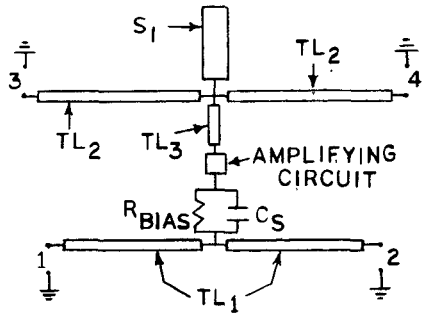

Fig. 12 Distributed amplifier gain section detail.

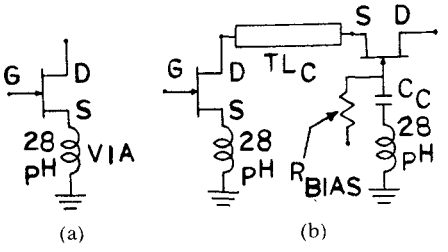

Fig. 13 Schematics of the amplifying circuits used in this study. (a) A common-source FET. (b) A cascode circuit

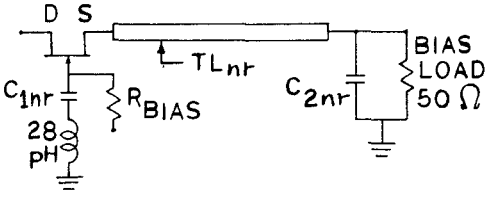

Fig. 14 The common-gate negative resistance circuit.

TABLE III
ELEMENT VALUES FOR THE FOUR-SECTION DA'S

	conventional	(input line) compensated	cascode	compenstd. cascode
TL_1 (microns)	w = 12.7 l = 128.2	w = 12.7 l = 98.6	w = 12.7 l = 99.6	w = 12.7 l = 98.3
TL_2 (microns)	w = 12.7 l = 168.8	w = 12.7 l = 155.0	w = 12.7 l = 128.1	w = 19.8 l = 149.6
TL_3 (microns)	w = 12.7 l = 120.0	w = 12.7 l = 65.0	(absent)	(absent)
S_1 (microns)	(absent)	w = 19.8 l = 18.5	(absent)	w = 35.0 l = 14.9
S_2 (microns)	(absent)	w = 19.8 l = 27.8	w = 35.0 l = 62.2	w = 19.8 l = 90.7
R_{st} (ohms)	(absent)	0 ohms, no loss	302	76
R_{bias} (ohms)	1000	1000	1000	1000
C_s (pF)	0.305	0.348	0.366	0.369
Common source FET amplifying circuit	60 micron FETs	60 micron FETs	(not utilized)	(not utilized)
Cascade amplifying circuit	(not utilized)	(not utilized)	60 micron FETs C_c = 3.0 TL_c: w = 12.7 l = 87.8	60 micron FETs C_c = 3.0 TL_c: w = 12.7 l = 340.0
Negative resistance compensat'n circuit -- input line	(not utilized)	90 micron FETs C_{1nr} = 2.5 C_{2nr} = 4.0 TL_{nr}: w = 12.7 l = 605.6	(not utilized)	90 micron FETs C_{1nr} = 3.0 C_{2nr} = 3.5 TL_{nr}: w = 12.7 l = 525.0

TABLE IV
ELEMENT VALUES FOR THE EIGHT-SECTION DA'S

	(input line) compensated	cascode	compensated cascode
TL_1 (microns)	w = 12.7 l = 103.1	w = 12.7 l = 95.0	w = 12.7 l = 101.3
TL_2 (microns)	w = 12.7 l = 154.9	w = 12.7 l = 99.5	w = 19.8 l = 147.7
TL_3 (microns)	w = 12.7 l = 19.6	w = 12.7 l = 17.5	w = 12.7 l = 4.3
S_1 (microns)	w = 19.8 l = 55.7	(absent)	w = 35.0 l = 26.9
S_2 (microns)	w = 19.8 l = 83.6	w = 35.0 l = 94.7	w = 19.8 l = 123.0
R_{st} (ohms)	0 (no loss)	226	50
R_{bias} (ohms)	1000	1000	1000
C_s (pF)	0.154	0.139	0.176
Common source FET amplifying circuit	60 micron FETs	(not utilized)	(not utilized)
Cascade amplifying circuit	(not utilized)	60 micron FETs C_c = 3.0 TL_c: w = 12.7 l = 118.9	60 micron FETs C_c = 3.0 TL_c: w = 12.7 l = 330.0
Negative resistance compensation circuit -- input line	90 micron FETs C_{1nr} = 2.5 C_{2nr} = 4.0 TL_{nr}: w = 12.7 l = 579.9	(not utilized)	90 micron FETs C_{1nr} = 3.0 C_{2nr} = 3.5 TL_{nr}: w = 12.7 l = 525.0

thickness 0.004 in and relative permittivity 12.9 was used in the simulations.

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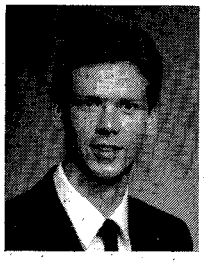

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